Amendments to the Claims

Listing of Claims - This will replace all prior listings of claims in the application:

1. (Currently Amended) An apparatus, comprising:

- a clock source to generate a clock signal;

- a first circuit, coupled to a first supply voltage source, to generate a first data signal and a second circuit coupled to a second supply voltage source;

- a flip-flop, having a pair of inputs coupled to the clock source and the first circuit, to generate a second data signal in response to the clock signal and the first data signal, with the flip-flop including a master latch and an upstream slave latch coupled to the master latch;

- a first level shifter, coupled to the flip-flop, to generate a level shifted data signal in response to the second data signal;

- a delay element coupled to the clock source and responsive to the clock signal to generate a delayed clock signal having a triggering clock edge and a non-triggering clock edge;

- a downstream slave latch, having an open state and a close state, a pair of inputs coupled to the first level shifter and the delay element and an output coupled to the second circuit, to generate an output data signal in response to the level shifted data signal and the delayed clock signal, with the triggering clock edge of the delayed clock signal switching the downstream slave latch from the close state to the open state; [[and]]

- a second level shifter, coupled between the clock source and the downstream slave latch and in series with the delay element, and

- wherein the level shifted data signal has a plurality of rising and falling data edges and the delay element is operable to delay an arrival of the triggering clock edge at the downstream slave latch until after an arrival of the rising and falling data edges at the downstream latch.

2. (Canceled)

3. (Currently Amended) The apparatus according to claim [[2]]1, wherein the delayed clock signal has a plurality of clock cycles with each of the clock cycles having a rising clock edge and a falling clock edge; and the triggering clock edge is selected from the rising clock edge and the falling clock edge, with a non-selected one of the rising clock edge and the falling edge being the non-triggerring clock edge.

4. (Currently Amended) The apparatus according to claim 1, wherein the delayed clock signal has a plurality of clock cycles with each of the clock cycles having a rising clock edge and a falling clock edge; and the downstream slave latch is switched from the close state to the open state by the triggering clock edge selected from the rising clock edge and the falling clock edge and switched from the open state to the close state by the non-selected clock edge of the rising clock edge and the falling clock edge.

5. (Canceled)

6. (Canceled)

7. (Previously Presented) The apparatus according to claim 4, wherein the level shifted data signal has a plurality of rising and falling data edges and the delay element is operable to introduce a predetermined delay having a duration exceeding a time period during which the rising and falling data edges are mismatched.

8. (Currently Amended) The apparatus according to claim 4, wherein ~~the flip-flop includes a~~the master latch is coupled to the clock source and [[an]]the upstream slave latch~~, having~~ has a pair of inputs coupled to the master latch and the clock source and an output coupled to the first level shifter~~, to generate the second data signal; and wherein the downstream latch being a downstream slave latch~~.

9. (Previously Presented) The apparatus according to claim 8, wherein the master latch has an input to receive the first data signal; and the flip-flop is operable to generate the second data signal in response to the first data signal.

10. (Currently Amended) An apparatus, comprising:

- a microprocessor including a central processing unit (CPU) section having a first supply voltage source; an input-output (I/O) section having a second supply voltage source; a clock source to generate a clock signal; and a selected section of the CPU section and the I/O sections being operable to generate a first data signal, with the selected section providing a first data signal;

- a converter circuit including a flip-flop, coupled to the clock source and the selected section, to generate a second data signal in response to the clock signal and the first data signal, with the flip-flop including a master latch and an upstream slave latch coupled to the master latch; a first level shifter, coupled to the selected section, to generate a level shifted data signal in response to the second data signal; a delay element and a second level shifter, coupled in series to the clock source, to generate a level shifted clock signal with a triggering clock edge and a non-triggering clock edge in response to the clock signal; a downstream slave latch having an open and a close state, a pair of inputs coupled to the first level shifter and the series-coupled delay element and second level shifter, and an output coupled to the non-selected section of the CPU and I/O sections; the downstream slave latch adapted to generate an output data signal in response to the level shifted data signal and the triggering clock edge of the level shifted clock signal; and

- wherein the level shifted data signal has a plurality of rising and falling data edges and the delay element is operable to delay an arrival of the triggering clock edge at the downstream slave latch until after an arrival of the rising and falling data edges at the downstream slave latch.

11. (Currently Amended) The apparatus according to claim 10, wherein the level shifted clock signal has a plurality of clock cycles with each of the clock cycles having a rising clock edge and a falling clock edge; the downstream slave latch has an open and a close state; and the downstream slave latch is switched from the close state to the open state by the triggering clock edge selected from the rising clock edge and the falling clock edge, with a non-selected one of the rising clock edge and the falling edge being the non-triggerring clock edge.

12. (Canceled)

13. (Canceled)

14. (Currently Amended) The apparatus according to claim 11, wherein ~~the flip-flop includes a~~the master latch is coupled to the clock source and [[an]]the upstream slave latch~~, having~~ has a pair of inputs coupled to the master latch and the clock source and an output coupled to the first level shifter~~, to generate the second data signal; and the downstream latch being a downstream slave latch~~.

15. (Previously Presented) The apparatus according to claim 14, wherein the master latch has an input to receive the first data signal; and the flip-flop is operable to generate the second data signal in response to the first data signal.

16. (Currently Amended) A system, comprising:

- a microprocessor including a central processing unit (CPU) section coupled to a first supply voltage source; an input-output (I/O) section coupled to a second supply voltage source; a clock source to generate a clock signal; and the CPU section being operable to generate a first data signal;

- a converter circuit including a flip-flop, coupled to the clock source and the selected section, to generate a second data signal in response to the clock signal and

the first data signal, with the flip-flop including a master latch and an upstream slave latch coupled to the master latch; a first level shifter, coupled to the CPU section, to generate a level shifted data signal in response to the second data signal; a delay element and a second level shifter, coupled in series to the clock source, to generate a level shifted clock signal having a triggering clock edge and a non-triggering clock edge in response to the clock signal; and a downstream slave latch having an open and a close state, a pair of inputs coupled to the first and second level shifters and an output coupled to the I/O section; the downstream slave latch being adapted to generate an output data signal in response to the level shifted data signal and the triggering clock edge of the level shifted clock signal;

- a source synchronous bus, coupled to the I/O section, to receive the level shifted data signal and the level shifted clock signal;

- an I/O module coupled to the source synchronous bus; and

- wherein the level shifted data signal has a plurality of rising and falling data edges and the delay element is operable to delay an arrival of the triggering clock edge until after an arrival of the rising and falling data edges at the downstream slave latch.

17. (Original) The system according to claim 16, wherein the I/O module is a selected one of a graphics and a video controller.

18. (Currently Amended) The system according to claim 16, wherein the level shifted clock signal has a plurality of clock cycles with each of the clock cycles having a rising clock edge and a falling clock edge; the downstream slave latch has an open and a close state; and the downstream slave latch is switched from the close state to open state by the triggering clock edge selected from the rising clock edge and the falling clock edge, with a non-selected one of the rising clock edge and the falling edge being the non-triggerring clock edge.

19. (Canceled)

20. (Canceled)

21. (Currently Amended) The system according to claim 18, wherein ~~the flip-flop includes a~~the master latch is coupled to the clock source and [[an]]the upstream slave latch~~, having~~ has a pair of inputs coupled to the master latch and the clock source and an output coupled to the first level shifter~~, to generate the second data signal; and the downstream latch being a downstream slave latch~~.

22. (Previously Presented) The system according to claim 21, wherein the master latch has an input to receive the first data signal; and the flip-flop is operable to generate the second data signal in response to the first data signal.

23. (Canceled)

24. (Canceled)

25. (Canceled)

26. (Canceled)

27. (Canceled)

28. (Currently Amended) A converter circuit, comprising

- a flip-flop including a master latch and an upstream slave latch, to generate a latched data signal in response to a clock signal and an input data signal; the flip-flop including a master latch and an upstream slave latch coupled to the master latch;

- a first level shifter, coupled to the flip-flop, to generate a level shifted data signal in response to the latch data signal, with the level shifted data signal having a plurality of signal transitions;

- a delay element to generate a delayed clock signal having a triggering clock edge and a non-triggering edge in response to the clock signal;

- a second level shifter, coupled in series with the delay element, to voltage level shift the delayed clock signal;

- a downstream slave latch having an open and a close state, coupled to the first level shifter and the delay element, to generate an output data signal in response to the level shifted data signal and the triggering clock edge; and

- wherein the delay element is adapted to delay an arrival of the triggering clock edge at the downstream slave latch until after an arrival of the signal transitions at the downstream slave latch.

29. (Canceled)

30. (Canceled)

31. (Currently Amended) The converter circuit according to claim [[30]28, wherein the delayed clock signal has a plurality of clock cycles with each of the clock cycles having a rising clock edge and a falling clock edge; and the downstream slave latch is switched from the close state to open state by the triggering clock edge, with the triggering clock edge being selected from the rising clock edge and the falling clock edge and a non-selected one of the rising clock edge and the falling edge being the non-triggerring clock edge.

32. (Currently Amended) The converter circuit, according to claim 28, ~~further comprising~~

~~- a second level shifter, coupled in series with the delay element, to voltage level shift the delayed clock signal: and~~

wherein the delay element is adapted to introduce a predetermined delay having a duration exceeding a time period during which the rising and falling data edges are mismatched.